

Fig. 1

002T90-0T5T6560

200

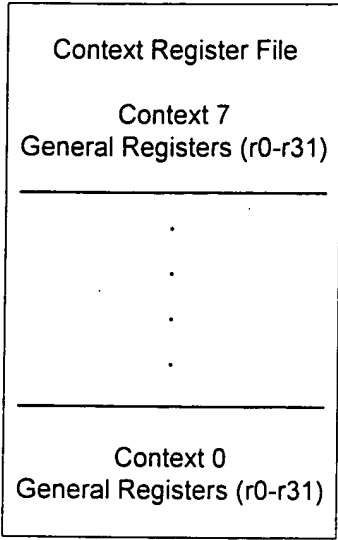


Fig. 2a

210

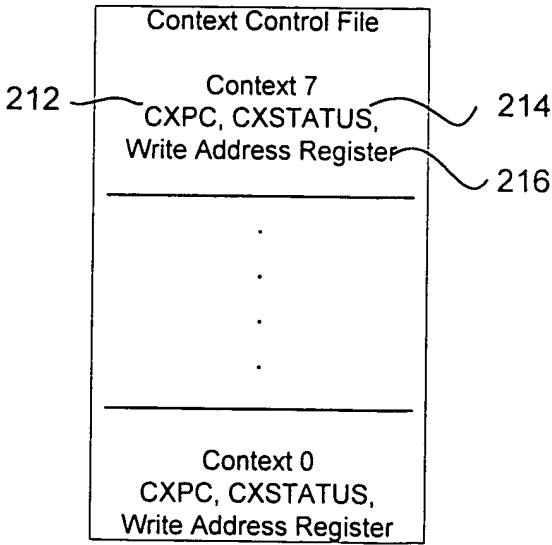


Fig. 2b

002T90" 0T5T6560

300

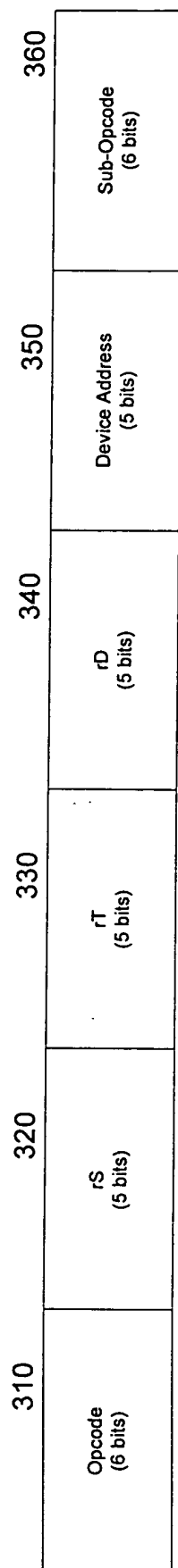


Fig. 3

Processor Fetches Instruction from Instruction
Memory Based on Processor Program Counter

420

Processor Forms a 64 Bit Descriptor
Concatenating Bits 63:32 of Register S (rS) with
Bits 31:0 of Register T (rT)

430

Processor Constructs System Bus Address
Using Device Address Provided in the
Instruction

440

Processor Initiates a System Bus Operation to
Write the Descriptor to the Device and
Requests that the Device Provide a Read Word
Response to an Identified Processor

450

Device Places Read Word on System Bus
Along with a Processor Identifier

460

Bus Controller Receives Read Word Response
From System Bus

470

Processor Writes Read Word to rD Register

Fig. 4

002150-01516560

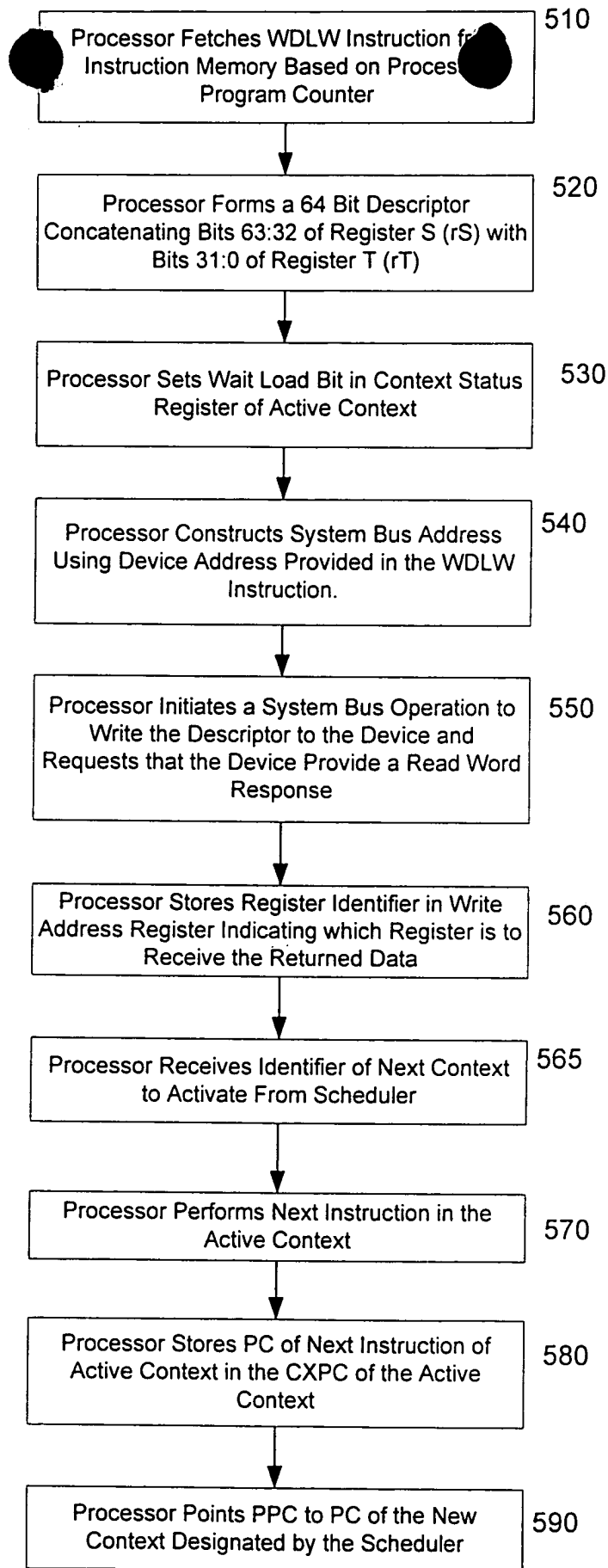


Fig. 5

002T90-0TST660

002790-061200

600

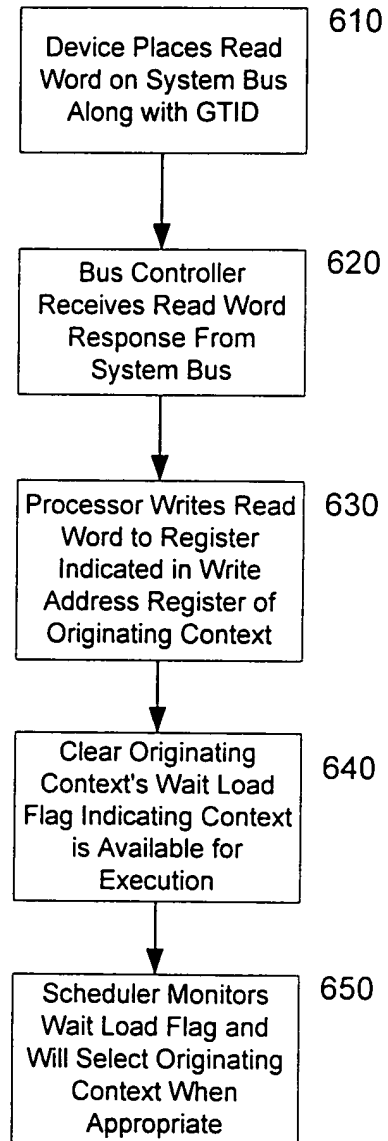


Fig. 6